REMARKS

Applicants acknowledge, with appreciation, the allowance of claims 1-33 and 40-56. In this Amendment, claims 40, 44, 46-49, 51, and 54 are amended to correct minor informalities in the claims. For the Examiner's convenience, an Appendix is attached showing the changes, in the format set forth in 37 C.F.R. § 1.121 for ordinary utility applications, between the allowed claims and the above listing of the claims. No new matter has been introduced.

Telephone Interview of July 9, 2010

Applicants thank Examiners Partridge and Padmanabhan for considering whether the above amendments to the claims are appropriate for entry under Rule 312. The amendments to claims 40, 44, 46-49, 51, and 54 were presented for consideration as listed above, except that claims 48, 49, and 51 were submitted for consideration as follows:

> 48. The processor of claim 47,
> wherein the instructions are ~~instruction sequence~~ is converted by a certain instruction conversion apparatus.
>
> 49. The processor of claim 48,
> wherein the instructions are ~~instruction sequence~~ is written in a high-level language before being converted by the instruction conversion apparatus.
>
> 51. The processor of claim 47,
> wherein at least a part of the instructions have a special bit which instructs the target processor to execute a plurality of ~~instruction~~ instructions in parallel.

In the amendment requested in pages 2-6 of this paper, the word "is" is deleted from claims 48 and 49, and the word "target" is deleted from claim 51. The Examiners indicated by telephone that entry of the proposed amendment appears to be acceptable, accompanied by the Examiners' suggestion that the term "target" in claim 51 also appeared to be appropriate for correction. Applicants have deleted the term "target" from claim 51 in view of the Examiners' suggestion.

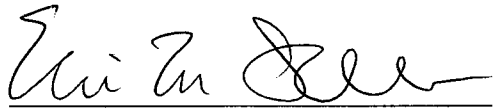
Conclusion

Applicants respectfully request the Amendment to be entered. If there are any questions regarding this Amendment, the Examiner is encouraged to contact Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX: REQUESTED CHANGES TO THE ALLOWED CLAIMS

40. A processor comprising:

an execution unit which executes up to N number of instructions having a variable bit length in parallel, N being an integer which is at least two, wherein the maximum bit length of an instruction that is executed in parallel is M bits, M being an integer;

an instruction supplying/issuing unit which fetches an instruction sequence in a unit of a first bit length of code and outputs the instruction sequence in a unit of a second bit length of code;

a decoding unit which decodes the instruction sequence in a unit of a variable bit length of code which is at least a part of the second bit length of code outputted by the instruction supplying/issuing unit, and outputting a decoding result to the execution unit; and

an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than M * N bits,

wherein the decoding unit decodes a plurality of instructions executed in parallel, and all of the instructions decoded in parallel at the same cycle pass through the instruction bus.

44. The processor of claim 40,

wherein at least a part of the instructions have a special bit which instructs the ~~target~~ processor to execute a plurality of instructions in parallel.

46. The processor of claim 40,

wherein the instruction supplying/issuing unit ~~comprising~~ comprises:

a fetch unit for successively fetching the instruction sequence; and

a plurality of instruction buffers for temporally storing instructions.

47. A processor comprising:

an instruction fetching unit that fetches instructions, each instruction having a variable bit length, wherein the maximum bit length of an instruction that is executed in parallel is M bits, M being an integer;

a decoding unit that decodes a plurality of instructions executed in parallel;

an execution unit that executes up to N number of decoded instructions from the decoding unit in parallel, N being an integer which is at least two; and

an instruction bus formed between the instruction fetching ~~supplying/issuing~~ unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than M * N bits,

wherein the total bit length of the decoded instructions that are executed in parallel is variable which is not related to the bit length of the fetched instructions, and all of the instructions decoded in parallel at the same cycle pass through the instruction bus.

48. The processor of claim 47,

wherein the instructions are ~~instruction sequence is~~ converted by a certain instruction conversion apparatus.

49. The processor of claim 48,

wherein the instructions are ~~instruction sequence is~~ written in a high-level language before being converted by the instruction conversion apparatus.

51. The processor of claim 47,

wherein at least a part of the instructions have a special bit which instructs the ~~target~~ processor to execute a plurality of ~~instruction~~ instructions in parallel.

54. The processor of claim 47,

wherein the instruction fetching unit ~~comprising~~ comprises:

a fetch unit for successively fetching the instruction sequence; and

a plurality of instruction buffers for temporally storing instructions.